

16/033340

Attorney Docket No.: 108298631US

CSG

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Date: January 6, 2005 By: Stephen P. Whelan
Stephen P. Whelan

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: BOON SUAN JEUNG *et al.*
PATENT NO.: 6,750,547 B2
ISSUED: JUNE 15, 2004
FOR: **MULTI-SUBSTRATE MICROELECTRONIC
PACKAGES AND METHODS FOR
MANUFACTURE**

EXAMINER: MAI-HUONG TRAN
ART UNIT: 2818
CONF. No.: 7237

Request for Certificate of Correction
under 37 C.F.R. §1.322 or §1.323

Certificate
JAN 14 2005
of Correction

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

1. The applicant(s) requests a Certificate of Correction to correct errors in the above-identified patent, which are listed on the enclosed Form PTO/SB/44.
2. Any errors on the part of the applicant are of a clerical or typographical nature or are otherwise minor in character. None of the requested corrections would constitute new matter or require reexamination of the patent.
3. Source of Error(s) and Payment of Fee:
 - ☒ All of the errors listed on Form PTO/SB/44 are believed to be due to mistake on the part of the USPTO (37 C.F.R. §1.322). Accordingly, no fees are believed to be due.
 - ☐ At least one of the errors occurred due to applicant's mistake made in good faith (37 C.F.R. §1.323).
 - ☐ A check covering the fee under 37 C.F.R. §1.20(a) (\$100.00) is enclosed herewith.

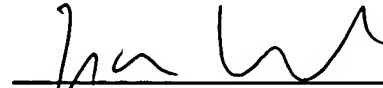
19 JAN 2005

☐ Please charge the fee under 37 C.F.R. §1.20(a) to Deposit Account No. 50-0665. This paper is provided in triplicate.

☒ Please charge any underpayment necessary for consideration of this paper to Deposit Account No. 50-0665.

4. Please send the Certificate of Correction to the undersigned at the address shown below.

Respectfully submitted,
Perkins Coie LLP



John M. Wechkin
Registration No. 42,216

Date: Jan 5, 2005

Correspondence Address:

Customer No. 25096
Perkins Coie LLP
P.O. Box 1247
Seattle, Washington 98111-1247
(206) 359-8000

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO : 6,750,547 *B2*

DATED : June 15, 2004

INVENTOR(S) : Boon Suan Jeung et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Front Page

Other Publications, please insert —US Application No. 09/981,948 Boon et al. Filed 10/16/01—;

Please delete duplicate entry of "EPIC CSP™ Chip Scale Package Technology, "Low Cost Area Array Package Fully Integrates Printed Circuit, Chip Interconnect and Assembly," EPIC Technologies, Inc., 30 pages.";

MAILING ADDRESS OF SENDER: Perkins Coie LLP
PATENT-SEA
PO Box 1247
Seattle, WA 98111-1247

PATENT NO. 6,750,547

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19 JAN 2005

UNITED STATES PATENT AND TRADEMARK OFFICE
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